Amendments to and Listing of the Claims:

This listing of claims replaces all prior versions and listings of the claims in the application. Please cancel claims 1, 4 and 5, amend claims 2 and 3 and add new claims 6 and 7 as follows:

1. (Cancelled).

2. (Currently Amended). A semiconductor device ~~having a plurality of read only storage devices which share an output data line and output data read from a memory cell in response to storage device selection information and address information, and a switching device wherein said switching device comprises:~~ for outputting data read from a read only storage device, comprising:

a plurality of read only storage devices, each read only storage device including memory cells;

a plurality of selecting signal lines for transmitting selecting signals to the plurality of read only storage devices, each selecting signal line being connected to a corresponding one of the plurality of read only storage devices, and each selecting signal indicating one of the plurality of read only storage devices storing data to be read;

an address signal line for transmitting an address signal to the plurality of said read only storage devices, said address signal indicating an address of memory cells storing data to be read; and

a switching device to which the selecting signals and the address signal are inputted, wherein said switching device comprises;

an address storage circuit for storing ~~said storage device selection information and said address information of a defective memory cell of at least one of said read only storage devices~~ address information of a defective memory cell of one of the plurality of read only storage devices and for detecting whether or not memory cells storing data selected by a selecting signal and an address signal include a defective memory cell;

a data storage circuit for storing ~~the~~ replacement data for memory cells including a ~~of~~ ~~said~~ defective memory cell, and outputting said replacement data in response to the detection of a defective memory cell by the address storage circuit; and

a switching circuit for inputting data outputted from memory cells of one of the plurality of the read only storage devices which is selected by a selecting signal and an address signal and replacement data outputted from the data storage circuit and outputting data outputted from one of the plurality of the read only storage devices which is not stored in memory cells including a defective memory cell and replacement data from said data storage circuit instead of data outputted from one of the plurality of read only storage devices which is stored in memory cells including a defective memory cell ~~which inputs the output data output from said read only storage device via said output data line and the output data from said data storage circuit, and outputs either of said two pieces of output data based on said storage device selection information and said address information stored in said address storage circuit~~.

3. (Currently Amended). A semiconductor device ~~having a plurality of read only storage devices, each of which includes a separate output data line and outputs data read from a memory cell in response to storage device selection information and address information, and a switching device wherein~~

~~said switching device comprises:~~ for outputting data read from a read only storage device, comprising:

a plurality of read only storage devices, each read only storage device including memory cells;

a plurality of selecting signal lines for transmitting selecting signals to the plurality of read only storage devices, each selecting signal line being connected to a corresponding one of the plurality of read only storage devices, and each selecting signal indicating one of the plurality of read only storage devices storing data to be read;

a plurality of address signal lines for transmitting address signals to the plurality of read only storage devices, each address signal line being connected to a corresponding one of the plurality of read only storage devices, and each address signal indicating an address of memory cells storing data to be read; and

a switching device to which the plurality of selecting signals and the plurality of said address signals are inputted,

wherein said switching device comprises:

an address storage circuit for storing ~~said storage device selection information and said address information of a defective memory cell of at least one of said read only storage devices~~ address information of a defective memory cell of one of the plurality of read only storage devices and for detecting whether or not memory cells storing data selected by a selecting signal and an address signal includes a defective memory cell;

a data storage circuit for storing ~~the~~ replacement data ~~of said defective memory cell~~ for memory cells including a defective memory cell and outputting said replacement data in response to the detection of a defective memory cell by said address storage circuit; and

a plurality of switching circuits ~~individually placed at each said output data line, which input the output data output from said read only storage device via said output data line and the output data from said data storage circuit, and output either of said two pieces of output data based on said storage device selection information and said address information stored in said address storage circuit~~, each switching circuit inputting data outputted from a corresponding one of the plurality of read only storage devices which is selected by a selecting signal and an address signal and replacement data outputted from said data storage circuit and each switching circuit outputting data outputted from a corresponding one of the plurality of read only storage devices which is not stored in memory cells including a defective memory cell and replacement data from said data storage circuit instead of data outputted from a corresponding one of the plurality of read only storage devices which is stored in memory cells including a defective memory cell.

4. (Cancelled).

5. (Cancelled).

6. (New). A semiconductor device for outputting data read from a read only storage device, comprising:

a read only storage device including memory cells;

an address signal line for transmitting an address signal to each read only storage device, said address signal indicating an address of memory cells storing data to be read; and

a switching device to which said address signal is inputted,

wherein said switching device comprises;

an address storage circuit for storing address information of a defective memory cell of said read only storage devices and for detecting whether or not memory cells storing data selected by an address signal includes a defective memory cell;

a bit storage circuit for storing bit information indicating which bit of data stored in memory cells including a defective memory cell is defective, and for outputting an inverted signal; and

a switching circuit for inputting said inverted signal and data outputted from a read only storage device which is selected by an address signal and for outputting said data from said read only storage device, said switching circuit inverting a defective bit of said data outputted from said read only storage device in response to receipt of an inverted signal from said bit storage circuit and outputting data whose defective bit is inverted instead of the data outputted from said read only storage device.

7. (New). A semiconductor device for outputting data read from a read only storage device, comprising:

a read only storage device including memory cells;

a rewritable storage device including memory cells and redundancy memory cells;

a plurality of selecting signal lines for transmitting selecting signals to said read only storage devices and said rewritable storage devices, each selecting signal line being connected to a corresponding one of said read only storage devices and said rewritable storage devices, each selecting signal indicating one of said read only storage devices and said rewritable storage devices, which stores data to be read;

a plurality of address signal lines for transmitting address signals to said read only storage devices and said rewritable storage devices, each address signal indicating an address of memory cells storing data to be read; and

a switching device to which the plurality of selecting signals and the plurality of address signals are inputted,

wherein said switching device comprises:

an address storage circuit for storing address information of a defective memory cell of a read only storage device or a rewritable storage device and for detecting whether or not memory cells storing data selected by a selecting signal and an address signal includes a defective memory cell;

a data storage circuit for storing replacement data for memory cells including a defective memory cell and for outputting said replacement data in response to the detection of a defective memory cell by said address storage circuit; and

a switching circuit for inputting data outputted from memory cells of a read only storage device which is selected by a selecting signal and an address signal and for inputting replacement data outputted from said data storage circuit and for outputting data outputted from said read only storage device which is not stored in memory cells including a defective memory cell and for outputting replacement data from said data storage circuit instead of data outputted from said read only storage device which is stored in memory cells including a defective memory cell and redundancy memory cells of said rewritable storage device instead of memory cells storing data selected by said selecting signal and said address signal which include a defective memory cell in response to the detection of a defective memory cell by said address storage circuit.